KERALA TECHNOLOGICAL UNIVERSITY

ERNAKULAM – I CLUSTER

DRAFT

SCHEME AND SYLLABI

FOR

M. Tech. DEGREE PROGRAMME

IN

VLSI & EMBEDDED SYSTEMS

(2015 ADMISSION ONWARDS)

SCHEME AND SYLLABI FOR M. Tech. DEGREE PROGRAMMEIN VLSI & EMBEDDED SYSTEMS

SEMESTER-1

Exam Slot	Course No:	Name	L- T – P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	06EC6015	CMOS Digital Design	4-0-0	40	60	3	4
B	06EC6025	Analog Integrated Circuit Design -1	4-0-0	40	60	3	4
C	06EC6035	Advanced Microcontrollers&Real Time Operating systems	4-0-0	40	60	3	4
D	06EC6045	Embedded System Design	3-0-0	40	60	3	3
E	06EC6x55	Elective I	3-0-0	40	60	3	3
F	06EC6065	Research methodology	0-2-0	100	0	0	2
G	06EC6075	Seminar I	0-0-2	100	0	0	2
H	06EC6085	VLSI& Embedded Systems Design LabI	0-0-3	100	0	0	1

Credits:23

	Elective I (06EC6x55)
06EC6155	VLSI Technology
06EC6255	Advanced Digital System Design
06EC6355	DSP Algorithms & Processors

SEMESTER-II

Exam Slot	Course No:	Name	L- T – P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	06EC6016	Analog Integrated Circuit Design -2	4-0-0	40	60	3	4
B	06EC6026	Embedded Product Design	3-0-0	40	60	3	3
C	06EC6036	VLSI Design Automation	3-0-0	40	60	3	3
D	06EC6x46	Elective II	3-0-0	40	60	3	3
E	06EC6x56	Elective III	3-0-0	40	60	3	3
F	06EC6066	Mini Project	0-0-4	100	0	0	2
G	06EC6076	VLSI& Embedded Systems Design LabII	0-0-3	100	0	0	1

Credits:19

Elective II - (06EC6x46)		Elective III- (06EC6x56)	
06EC6146	System on chip Design	06EC6156	Embedded Linux systems
06EC6246	FPGA Architecture & Applications	06EC6256	Modeling of Embedded Systems
06EC6346	VLSI Architectures for DSP	06EC6356	Mobile Handset Architecture

SEMESTER-III

Exam Slot	Course No:	Name	L- T – P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	06EC7x15	Elective IV	3-0-0	40	60	3	3
B	06EC7x25	Elective V	3-0-0	40	60	3	3
C	06EC7035	Seminar II	0-0-2	100	0	0	2
D	06EC7045	Project(Phase 1)	0-0-8	50	0	0	6

Credits: 14

Elective-IV**(**06EC7x15**)**		Elective-V**(**06EC7x25**)**	
06EC7115	High Speed Digital Design	06EC7125	Low Power Digital Design
06EC7215	MEMS & Micro system Design	06EC7225	VLSI System Testing
06EC7315	DSP Architecture and Design	06EC7325	Memory Design & Testing

SEMESTER-IV

Exam Slot	Course No:	Name	L- T – P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (hrs)	
A	06EC7016	Project (Phase 2)	0-0-21	100	0	0	12

Credits: 12

Total Credits for all semesters: 68

SEMESTER - I

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6015	CMOS DIGITAL DESIGN	4-0-0-4		2015

Course Objectives

1. To learn concepts of VLSI Design flow
2. To learn CMOS based static circuits and dynamic circuits, Delay analysis.
3. To learn how to design static and dynamic circuits by using different CMOS logic families
4. To learn Datapath subsystem design- Different arithmetic circuits
5. To learn Memory elements and memory system design

Syllabus

Fundamentals of CMOS basic gates design. Different types of static and dynamic circuits. Delay and power analysis of VLSI circuits. Different Datapath systems-Adders multipliers-Shifters\Rotator. Case studies on datapath systems. Design and analysis of memoy elements and memory systems.

Course Outcome

Students who successfully complete this course will demonstrate an ability to design CMOS systems and will be able to make the layout of the system using a suitable tool. Students will be able to analyse the power and delay of CMOS circuits. Should get an idea about different dynamic CMOS families. Students will acquire knowledge on different arithmetic circuits- Adders multipliers-Shifter\Rotator circuits and different memory systems.

Text Books

1. Weste and Harris, “CMOS VLSI Design: A circuits and systems perspective”, 4/e, 2011, Pearson Education
2. John Paul Uyemura, "Introduction to VLSI circuits and systems", Wiley India Pvt. Limited.
3. Rabaey, Chandrakasan and Nikolic, “Digital Integrated Circuits – A Design Perspective”, 2/e, Pearson Education
4. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits, 3/e, Tata McGraw-Hill Education, 2003
5. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.

Course Plan

Module	Content	Hours	Sem. Exam Marks

I	Static Circuits and interconnects:- Static Circuits, CMOS Inverter - DC Characteristics, Noise Margin, Beta Ratio Effects , CMOS NAND, NOR and Complex Gates , Pass Transistor- DC Characteristics. Delay models- Definition, Transient Response, RC Delay Model: Effective Resistance, Gate and Diffusion Capacitance, Equivalent RC Circuits ,Elmore Delay Model: Layout Dependence of Capacitance, Determining Effective Resistance, Linear Delay Model: Logical Effort, Parasitic Delay, Delay in a Logic Gate Drive, Logical Effort of Paths: Delay in Multistage Logic Networks, Choosing the Best Number of Stages, Limitation of Logical Effort. Interconnects -Wire Geometry, Intel Metal Stacks, Interconnect Modeling: Resistance, Capacitance, Inductance, Skin Effect, Interconnect Engineering: Width, Spacing and Layer, Repeaters, Crosstalk Control, Regenerators, Logical Effort with Wires.	14	25
II	Dynamic circuits - Dynamic circuits Fundamentals of dynamic logic: Charge Sharing, Charge Leakage, Dynamic Circuits: pitfalls, pass transistor circuits.	14	25
	INTERNAL TEST 1		
	Alternate CMOS logic-Domino CMOS, Multi Output Domino Logic, Dual-rail Domino Logic, NP Domino logic(NORA), True-Single-Phase-Clock(TSPC) CMOS logic, Power dissipation in CMOS circuits. BiCMOS Circuits: Working.		
III	Sequential Design Circuit Design of Latches and Flip-Flops- Conventional CMOS Latches and FF ,Pulsed Latches , Resettable Latches and FFs, Enabled Latches and FFs, Incorporating Logic into Latches , Klass Semi Dynamic FF, Differential FF, Dual Edge Triggered FF , TSPC Latches and FF . Low power sequencing elements- State Retention Registers , Level Converter Flip Flops, Static Sequencing Element Methodology - Choice of Elements ,Characterizing Sequencing Element Delays , Sequencing static circuits - Sequencing Methods: FF, Latches, Pulsed Latches , Max Delay Constraints , Min Delay Constraints , Time Borrowing. Clocks - Definitions, Global Clock Generation: PLL, DLL Formulation, Global Clock Distribution. Synchronization - Metastability, Synchronizers: simple synchronizer.	12	25

	INTERNAL TEST 2		
IV	Datapath and Memory Subsystems: - Data path subsystems – Design Considerations , The Binary Adder: Definitions, The Full Adder: Circuit Design Considerations The Binary Adder: Logic Design Considerations, Generation, Partial Product Accumulation, final Addition , Shifters: Barrel Shifter, Logarithmic Shifter. Memory Subsystems - SRAM: Cells ,Row Circuitry, Column circuitry, Low-power SRAMs, Case Study1- Logarithmic Adders, Case Study2 - Advanced Memory Types: QDR SDRAM, MRAMs, RRAMs.	12	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6025	Analog Integrated Circuit Design -1	4-0-0-4		2015

Course Objectives

To give the Student an idea about:-

1. The operation of the MOS transistor
2. Understand the behaviour of the MOS transistor in circuits
3. Understand how MOS transistors are modelled for CAD tools
4. The analysis of the Single stage amplifiers

Syllabus

Operation and modeling of MOS transistor; Short channel effects and modelling of MOS devices; Noise and frequency response analysis of single stage amplifiers.

Course Outcome

Students who successfully complete this course will be able to analyze quantitatively the behaviour of MOS transistor in various regions of operation; use the time domain and frequency domain concepts in analysing the circuits; to design a CMOS based system, component, or process within realistic constraints.

Text Books

1. YannisTsividis and Colin McAndrew , "Operation and Modeling of the MOS Transistor", 3/e, 2010, OUP .
2. R. Jacob Baker, Harry W Li, David E Boyce, " CMOS – Circuit Design, Layout, and Simulation",3rd Edition, 1998.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill 2008.
4. Philip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design" International Student(Second) Edition, First Indian Edition 2010.

Course Plan

Module	Content	Hours	Sem. Exam

			Marks
I	**2-Terminal MOS Structure** - Flat Band Voltage, Potential Balance and Charge, Effect of Gate-Body Voltage on Surface Condition General Analysis. Inversion: charge sheet approximation, Strong and Weak Inversion, Small Signal Capacitance. **3-Terminal MOS Structure** - Contacting Inversion Layer, General Analysis, Body-effect, Pinch-off voltage. Introduction, Regions of Operation.	14	25
II	**4-Terminal MOS Structure** – Introduction, Complete All-Region Model – Current Equations, Simplified All-Region Models: Linearizing Depletion Region Charge, Source-Referenced Simplified All- Region Models.	14	25
	INTERNAL TEST 1		
	Strong Inversion: Complete Strong Inversion Model-NonSaturation, Source-Referenced Simplified Strong Inversion Models		
III	**Short Channel Effects**: Scaling Theory, Threshold Voltage Variation, Mobility Degradation with Vertical Field, Velocity Saturation, Hot Carrier Effects. **MOS Device Models**: Level 1 Model, Level 2 Model, Level 3 Model , BSIM Series, Other Models, Charge and Capacitor Modeling, Temperature Dependence. **Noise**: Statistical Characteristics of Noise, Noise Spectrum, Amplitude Distribution, Correlated and Uncorrelated Sources. Types of Noise: Thermal, Flicker, Shot Noise Representation of Noise in Circuits.	12	25
	INTERNAL TEST 2		
IV	**Single-Stage Amplifiers** - Introduction to basic amplifier Configurations - Resistive Load **Active Loads**: Gate-Drain Connected Loads: CS, CD and CG, Frquency Response, Noise Analysis, Current-Source Load: CS, CD and CG, Frequency Response, Noise Analysis,	12	25

	Cascode, Folded Cascode, Push-pull amplifier- Noise Analysis		
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6035	**ADVANCED MICROCONTROLLERS AND REAL TIME OPERATING SYSTEMS**	**4-0-0-4**		**2015**

Pre-requisites: Knowledge about the architecture of an 8bit micro controller will be an advantage

Course Objectives

5. To learn the architectural features of the popular ARM micro controller
6. To learn the concepts of Real Time Operating Systems and the various features of RTOS
7. To have the concepts for the software development for embedded systems

Syllabus

Architecture and features of ARM11 micro controller, Design considerations for Power saving modes, Real Time Operating System Concepts and architecture, RTOS features, Scheduling concepts, Concepts of the software development process for Embedded Systems, Embedded System Software development flow, General concepts for writing embedded programs, Case study to familiarize the design aspects of embedded systems involving Real Time Operating Systems

Course Outcome

Students who successfully complete this course will be having the knowledge about the ARM micro controller architecture and its features. Students should be able to contribute the knowledge in the design of ARM micro controller based embedded systems. Students will also be able to understand the various features of Real Time Operating Systems and its use in Embedded Systems. Students will be able to involve in the Embedded software design process involving RTOS with the help of the concepts discussed in the syllabus and will also get an opportunity to do case study on the representative embedded systems discussed, to better understand the concepts.

Text Books

1. David Seal, "Arm Architecture Reference Manual", 2nd Edition Addison-Wesley, 2000
2. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", 3rd Edition Newnes Publishers, 2013.
3. Dr. K V K K Prasad, "Embedded/Real Time Systems: Concepts, Design and Programming Black Book", DreamTech Press, 2003.

References

1. Philip A Laplante, "Real-Time Systems Design and Analysis: An Engineer's Handbook", 4th Edition, Wiley.

2. Raj Kamal, "Embedded Systems Architecture, Programming and Design", 2nd Edition, Tata McGraw-Hill, 2008.

3. Robert Oshana,DSP for Embedded and Real-Time Systems, Newnes, 2012.

4. BorkoFurht, Dan Grostick, David Gluch, Guy Rabbat, John Parker, Meg McRoberts, "Real-Time UNIX® Systems: Design and Application Guide"Springer, 2012 .

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Introduction to ARM processor family, ARM-11- Architectural features- Instruction and pipeline stages-Coprocessor–Memory management-TLB organization-Modes of operation-Exception handling-Interrupts: Nested and non-nested-Interrupt handling schemes-Debug systems-Design considerations for Power saving modes.	14	25
II	Introduction to RTOS-Concept-Comparison of RTOS and General Purpose Operating Systems-RTOS Architectures: Round Robin, Round Robin with interrupts, Function Queue scheduling Architecture, Architecture selection, Kernel functions, POSIX standard, Task and task states, Priorities, Task scheduling, Inter task communication, Semaphore and shared data, Message Queues, Mail boxes and pipes, Timer functions, events.	14	25
	INTERNAL TEST 1		
	Memory Management, Interrupt routine in an RTOS environment. Hard real time scheduling considerations, saving memory space, saving power.		
III	Software development for Embedded Systems: The compilation process, Native versus cross compilers, Host and Target Machines, Linker/ Locator for Embedded Software , Getting Embedded Software into the target system, Debugging Techniques-Testing on your host machine, Instruction set Simulators, Porting Kernels, C extensions for Embedded Systems, Downloading, Emulation and Debugging Techniques. Buffering and other data structures: Double buffering, buffer exchanging, Linked lists, FIFO, Circular buffers, Buffer under run and overrun, memory leakage, Memory and performance tradeoffs, Board Support Packages.	12	25
	INTERNAL TEST 2		

IV	RTOS Case studies-Traffic light system- Software performance engineering of an embedded system DSP application- Data acquisition system-Smart card –Aviation control -Radio Control.	12	25
END SEMESTER EXAM			

Course Code	**Course Name**	**L-T-P-C**		**Year of Introduction**
06EC6045	**EMBEDDED SYSTEM DESIGN**	**3-0-0-3**		**2015**

Course Objectives

1. To learn about Embedded systems, its design challenges and optimization
2. To learn the concepts of Processor Design and memory design
3. To have the concepts of control systems

Syllabus

Embedded system overview, Design challenges, Optimization, Processor and IC technology, Processor design, Memory Design, Control Systems.

Course Outcome

Students who successfully complete this course will be having the knowledge about embedded systems, its design challenges and the various optimization techniques. Students should be able to contribute the knowledge in the design of embedded systems. Students will also be able to understand about processor design, memory design and control systems.

Text Book

1. Frank Vahid, Tony D. Givargis, "Embedded System Design – A Unified Hardware/ Software Introduction", John Wiley and Sons, Inc 2002.

References

1. Jonathan W. Valvano, "Embedded Microcomputer systems", Brooks / Cole, 3rd Edition CENGAGE Learning, 2012.
2. Steve Heath, ButterworthHeinemann, "Embedded Systems Design", Newnes, 1997
3. Gajski and Vahid,"Specification and Design of Embedded systems",Prentice Hall, 1994
4. Timothy J. Ross, "Fuzzy Logic with Engineering Applications", 3rd Edition, Wiley, 2010.
5. M Ganesh, "Introduction to Fuzzy Sets and Fuzzy Logic", Prentice Hall India,2006

Course Plan

Module	Content	Hours	Sem. Exam Marks

I	Embedded system overview, Design challenge: Optimizing design metrics, Processor Technology, General purpose Processors, Single purpose Processors, and Application Specific Processors, IC Technology: Full custom/ VLSI, Semicustom ASIC, PLD, Trends, Design Technology.	10	25
II	Processor Design: Custom Single purpose Processor: RT level combinational components, RT level sequential components, Custom Single purpose Processor Design, RT level Custom Single purpose Processor Design, Optimizing Custom Single purpose Processors, Optimizing the original program, Optimizing the FSMD, Optimizing the datapath, optimizing the FSM. General purpose Processors: Basic architecture, Datapath, Control unit, Memory, Pipelining	10	25
	INTERNAL TEST 1		
	Superscalar and VLIW architectures. Application Specific instruction set Processors (ASIP's), Microcontrollers, DSP, Less General ASIP environments, Selecting a Microprocessor/ General purpose Processor		
III	Memory Design: Memory devices used in microcontroller based embedded systems, timing diagrams-read and write operations-burst read/write devices, Composing memory, Cache design-cache mapping and replacement policies, cache write techniques. Basic protocol concepts, ISA bus protocol, Serial protocols and Parallel protocols.	10	25
	INTERNAL TEST 2		
IV	Control Systems: Open-loop and closed –loop control systems, an open-looped automobile cruise controller, a closed-loop automobile cruise controller, General control systems and PID controllers, Control objectives, Modeling real physical systems, Controller design, Fuzzy control, Practical Issues Related to Computer based Control, Benefits of Computer Based Control Implementations.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6155	VLSI TECHNOLOGY	3-0-0-3		2015

Course Objectives

1. To learn VLSI process and get an idea about clean room requirements
2. To learn about different impurity incorporation techniques and models.
3. To learn descriptions and models of different processing steps

Syllabus

Introduction to clean room requirements, Wafer cleaning, Diffusion models, Oxidation , Lithography, Chemical vapour deposition, Metallization.

Course Outcome

At the end of the course, student will know the details of VLSI processing steps, Different diffusion models. Student will acquire knowledge on oxidation, Lithography, Chemical vapour deposition and metallization.

Text Book

1. S.M.Sze (Ed), "VLSI Technology", 2nd Edition, McGraw-Hill, 1988.
2. B.G Streetman, “VLSI Technology” , Prentice Hall, 1990.
3. C.Y. Chang and S.M. Sze (Ed), "ULSI Technology", McGraw-Hill Companies Inc.,1996.
4. S.K.Gandhi, "VLSI fabrication Principles”, John Wiley Inc., New York, 1983.
5. Sorab K. Gandhi, “The Theory and Practice of Microelectronics”, John Wiley & Sons 1968.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Environment for VLSI technology: clean room and safety requirements, Wafer Cleaning process and wet chemical etching techniques. Impurity incorporation: solid-state diffusion modeling and technology, Ion implantation: modeling, technology and damage annealing; Characterization of impurity profiles.	10	25

II	Oxidation: kinetics of silicon dioxide growth for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; high K and low K dielectrics for ULSI.	10	25
	INTERNAL TEST 1		
	Lithographic techniques: Photolithography techniques for VLSI/ULSI; Mask generation.		
III	Chemical Vapour deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; epitaxial growth of silicon; modeling and technology.	10	25
	INTERNAL TEST 2		
IV	Metalisation techniques: evaporation and sputtering techniques. Failure mechanisms in metal interconnects; multilevel Metalisation schemes. Masking Sequence and Process flow for MOS and BIPOLAR Devices. Topological Design rules.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6255	ADVANCED DIGITAL SYSTEMS DESIGN	3-0-0-3		2015

Course Objectives

To enable the students

1. To understand the concept of standard combinational and sequential modules, programmable devices and modular approach
2. To learn the analysis and design concepts of synchronous and asynchronous digital systems and implement using different standard modules.
3. To identify the relevance of timing issues and solutions in digital systems.

Syllabus

Standard combinational MSI and LSI modules and modular networks, Synchronous Sequential Circuit Design, Finite State Machine design procedure Standard sequential modules and modular networks, Asynchronous sequential circuits, Timing Issues in Digital System Design, Design of combinational logic using programmable devices.

Course Outcome

Students will be able to understand the concepts of Standard combinational and sequential MSI and LSI modules, programmable devices and design modular networks, learn the analysis and design procedure of combinational systems, synchronous and asynchronous finite state machines and implementation of these systems using standard modules.

Students will also be able to assess the relevance of various timing issues and synchronization methods in digital systems.

Text Book

1. Charles H Roth- Fundamentals of Logic Design, 5th ed,Cengage Learning,2004.
2. Milos D Ercegovac, Tomas Lang- Digital Systems and Hardware/Firmware Algorithms, John Wiley,1985

References

1. William Fletcher- A systematic Approach to Digital Design, PHI, 1996
2. N NBiswas- Logic Design Theory, PHI, 1993
3. Jan M. Rabaey, A Chandrakasan, B. Nikolic- Digital Integrated Circuits- A

DesignPerspective, 2nd Edition, PHI/Pearson, 2003

4. ZviKohavi- Switching and Finite Automata Theory, Tata McGraw Hill, 1978
5. Comer- Digital Logic State Machine Design, 3rd Edition, Oxford University Press, 1995

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Standard combinational MSI and LSI modules and modular networks: Arithmetic circuits, comparators, Multiplexers, Decoders, Code converters, ROMs, cost, speed and reliability comparison aspects of modular networks, XOR and AOI gates.Design of combinational logic using PAL and PLA, Implementation of switching functions using FPGA	10	25
II	Synchronous Sequential Circuit Design: Clocked Synchronous State Machine Analysis,Mealy and Moore machines, Finite State Machine design procedure – derive state diagrams and state tables, state assignments, state reduction methods. Implementing the states of FSM using different FFs, Incompletely specified state machines.	10	25
	INTERNAL TEST 1		
	Standard sequential modules and modular networks:- State register/Counters with combinational networks. ROMs and combinational networks in FSM design,Multimodule implementation of counters- cascade and parallel, multimodule registers.		
III	Asynchronous sequential circuits:- Analysis- Derivation of excitation table, Flow table reduction, state assignment, transition table, Design of Asychronous Sequential Circuits, Race conditions and Cycles, Static and dynamic hazards, Methods for avoiding races and hazards, Essential hazards.Designing with SM charts – State machine charts, Derivation of SM charts, and Realization of SM charts.	10	25
	INTERNAL TEST 2		
IV	Timing Issues in Digital Sytem Design:- Timing classifications, skew and jitter, latch based clocking, selftimed circuit design- self timed logic, completion signal generation, self timed signaling, synchronizers and arbiters. Sequential circuit design using PLAs, CPLDs, FPGAs.	10	25

END SEMESTER EXAM

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6355	DSP ALGORITHMS & PROCESSORS	3-0-0-3		2015

Course Objectives

To give the student:-

1. An introduction to various advanced architectures of DSP processors
2. Practice in the programming of DSP processors.

Syllabus

Fundamentals of DSP architecture; various architectures of processors; DSP benchmarks, Pipeline implementation; Instruction level parallelism; review of memory hierarchy; TMS320C6x DSP processor: architectural details; addressing modes; instruction set; peripherals; SHARC processor: architectural details, peripherals.

Course Outcome

Upon completion of this course student will be able to Understand various advanced architectures of DSP processors and DSP benchmarks; Learn the role of pipelining and parallelism in DSP processors; Understand the architectural details of TMS320C6x processor and SHARC processor; Apply the instructions of TMS320C6x processor in assembly and C programming.

Text Book

1. Steven W Smith, Digital Signal Processing: A Practical guide for Engineers and scientists, Newness (Elsevier), 2003.
2. RulfChassaing, Digital Signal Processing and applications with the C6713 and C6416 DSK, Wiley- Interscience, 2005.

References

1. Sen M Kuo, Bob H Lee, Real time Digital Signal Processing, , John Wiley and Sons, 2001.

2. Nasser Kehtarnawaz, Real Time Signal Processing Based on TMS320C6000, Elsevier,2004.

3. JL Hennesy, D.A. Patterson, Computer Architecture A Quantitative Approach; 3rd Edition, Elsevier India, 2011

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Introduction: Need for special DSP processors, Von Neumann versus Harvard Architecture, Architectures of superscalar and VLIW fixed and floating point processors, review of Pipelined RISC, architecture and Instruction Set Design, Performance and Benchmarks- SPEC CPU 2000, EEMBC DSP benchmarks. Basic Pipeline: Implementation Details- Pipline Hazards.	10	25
II	Instruction Level Parallelism (ILP): Concepts, dynamic Scheduling - reducing data hazards. Tomasulo algorithm, Dynamic Hardware Prediction- reducing Branch Hazards	10	25
	INTERNAL TEST 1		
	Multiple Issue- hardware-based Speculation, limitations of ILP, review of memory hierarchy – Cache design, cache Performance Issues, improving Techniques.		
III	TMS 320 C 6x: Architecture, Functional Units, Fetch and Execute Packets, Pipelining, Registers, Linear and Circular Addressing Modes, Indirect Addressing, Circular Addressing,TMS320C6x Instruction Set, Types of Instructions, Assembler Directives, Linear Assembly, ASM Statement within C, C-Callable Assembly Function, Timers, Interrupts, Multichannel Buffered Serial Ports, Direct Memory Access, Memory Considerations, Fixed- and Floating-Point Formats, Code Improvement, Constraints.	10	25
	INTERNAL TEST 2		
IV	SHARC Digital Signal Processor: – Architecture, IOP Registers, peripherals, synchronous Serial Port, interrupts, internal/external/multiprocessor memory space, multiprocessing, host Interface, link Ports. Review of TMS 320 C 6x and SHARC digital signal processors based on DSP bench marks.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6065	**RESEARCH METHODOLOGY**	0-2-0-2		**2015**

Course Objectives

The primary objective of this course is to develop a research orientation among the scholars and to acquaint them with fundamentals of research methods. Specifically, the course aims at introducing them to the basic concepts used in research and to scientific social research methods and their approach. It includes discussions on sampling techniques, research designs and techniques of analysis. Some other objectives of the course are:

1. To develop understanding of the basic framework of research process.
2. To develop an understanding of various research designs and techniques.
3. To identify various sources of information for literature review and data collection.
4. To develop an understanding of the ethical dimensions of conducting applied research.
5. Appreciate the components of scholarly writing and evaluate its quality.

Syllabus

Research methodology; Research Process; Application of results , ethics and intellectual property rights; Techniques of developing measurement tools; Processing and analysis of data; Interpretation and report writing-techniques of interpretation; Graphic & diagrammatic representation data; Defining research problem ; Experimental Designs; Sampling fundamentals; Testing of hypotheses.

Course Outcome

At the end of this course, the students should be able to:

- Understand some basic concepts of research and methodologies.
- To Identify appropriate research topics.
- Select and define appropriate research problem and parameters.
- Prepare a project proposal (to undertake a project) .
- Organize and conduct research (advanced project) in a more appropriate manner.
- Write a research report and thesis.
- Write a research proposal (grants).
- Attain basic knowledge of experimentation methods and statistical analysis.

Text Book

1. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., An introduction to Research Methodology, RBSA Publishers. 2002.
2. Kothari, C.R., Research Methodology: Methods and Techniques. New Age International. 1990.
3. Deepak Chawla and NeenaSondhi Research Methodology concepts and cases Vikas Publishing house pvt ltd, 2011
4. R. Paneerselvam , Research Methodology, PHI Learning, 2014
5. Sinha, S.C. and Dhiman, A.K., Research Methodology, EssEss Publications. 2 volumes., 2002.

6. Trochim, W.M.K., Research Methods: the concise knowledge base, Atomic Dog Publishing. 2005.
7. Wadehra, B.L. Law relating to patents, trade marks, copyright designs and geographical indications.Universal Law Publishing, 2000.
8. Day, R.A., How to Write and Publish a Scientific Paper, Cambridge University Press, 1992..
9. Fink, A., Conducting Research Literature Reviews: From the Internet to Paper. Sage Publications, 2009.
10. Leedy, P.D. and Ormrod, J.E., Practical Research: Planning and Design, Prentice Hall, 2004

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Research methodology: meaning of research, objectives, type of research approaches, researchprocess, and criteria for good research. Concept of theory, empiricism, deductive and inductivetheory. Characteristics of scientific method – Understanding the language of research – Concept,Construct, Definition, Variable. Research ProcessApplication of results and ethics - Environmental impacts - Ethical issues - ethical committees -Commercialization – Copy right – royalty - Intellectual property rights and patent law – TradeRelated aspects of Intellectual Property Rights – Reproduction of published material – Plagiarism -Citation and acknowledgement - Reproducibility and accountability.	10	25
II	Techniques of developing measurement tools – scaling – important scaling techniques. Methods ofdata collection–collection of primary data–observation method questionnaires –other methods ofdata collection. Processing and analysis of data – processing operations – editing – coding –classification – tabulation. Interpretation and report writing-techniques of interpretation – steps inreport writing.	10	25
	INTERNAL TEST 1		
	Graphic & diagrammatic representation data - Purpose of Diagrams & Graphs, Bar diagrams(Simple, Component & Percentage), Pie Charts, Line Square Diagrams, Interpretations &Comparisons, Graphical Representation of Frequency Distribution, Histograms, FrequencyPolygon, Frequency Curve.		

III	Defining research problem – research design, features of good design - different research designsbasicprinciple of experimental design developing a research plan.Experimental Designs - purpose of designing experiments, methods of increasing accuracy ofexperiments, replication, control & randomization and their objectives & advantages - basic ideasof completely randomized , randomized block, Factorial and Latin square designs.	10	25
	INTERNAL TEST 2		
IV	Sampling fundamentals – need for sampling – important sampling distribution: Samplingdistribution of mean- sampling distribution of proportion – student's 't' distribution – F distribution–Chi-square distribution – concept of standard error - – sample size and its determination.Testing of hypotheses – procedure for testing hypotheses - important parametric tests: Z test, t-test,chi- square test, F test and ANOVA. Softwares for statistical testing.	10	25
END SEMESTER EXAM			

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC6075	SEMINAR I	0-0-2-2	2015

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC6085	VLSI& EMBEDDED SYSTEMS DESIGN LAB I	0-0-3-1	2015

Digital Circuit Design

Hardware modelling of Combinational and Sequential circuits using Verilog/VHDL

Verification of the logic using test bench

Design, implementation and verification on FPGAs

Analog Circuit Design

Device characterization, Spice analysis of CS, CG and CD amplifiers

Embedded Design

Familiarization of microcontroller based development platform through application development

RTOS functions, RTOS porting to a suitable micro controller.

SEMESTER-II

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6016	Analog Integrated Circuit Design -2	4-0-0-4		2015

Course Objectives

1. To give the Student an idea about:-
2. The state-of-the-art review of the principles, concepts and techniques required to produce successful designs of analog integrated circuits using CMOS technologies.
3. Analysis of various circuits such as current mirrors, differential amplifiers and op amps.
4. Analysis of switched capacitor circuits, basics of Data converters.

Syllabus

Analysis of various current mirror structures, differential mplifiers and Operational Amplifiers; Comparator design and data converter types, switched capacitor types.

Course Outcome

Students who successfully complete this course will be able to design and simulate analog circuits using spice, and analyze problems related to fabrication of analog ICs; an ability to design a CMOS based system, component, or process within realistic constraints; an ability to use the techniques, skills, and modern tools necessary for CMOS based circuit design.

Text Books

1. R. Jacob Baker, Harry W Li, David E Boyce, " CMOS – Circuit Design, Layout, and Simulation",3rd Edition, 1998.
2. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill 2008.
3. Philip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design" International Student(Second) Edition, First Indian Edition 2010

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Current Mirrors- Simple MOS Current Mirror: Sensitivity Analysis, Temperature Analysis, Transient Response. Cascode Current Mirror -Band Gap References, Supply Independent Biasing, Temperature Independent References, PTAT Current Generation, Constant Gm Biasing	14	25
II	CMOS Differential Amplifiers Introduction, Basic Differential Pair – Analysis, Common Mode Response, Differential Pair with MOS Loads, Frequency Response, Noise Analysis.	14	25

	INTERNAL TEST 1		
	CMOS Operational Amplifiers: Operational Transconductance Amplifiers (OTA), One stage and two stage operational amplifiers, Gain Boosting , Common Mode Feedback, Cascode and Folded Cascode Structures, Stability Analysis, Introduction to compensation techniques.		
III	**CMOS Comparators-** Characterization of a comparator ,Two stage open loop comparators, Other Open loop Comparatos - Push-pull output comparator, comparators capable of driving very large capacitive loads **CMOS Data Converters** - Basics of CMOS Data Converters-Medium and High speed CMOS Data converters Over sampling Converters.	12	25
	INTERNAL TEST 2		
IV	Switched Capacitor Circuits-Switched capacitor amplifiers, Switched capacitor integrators, First and Second Order Switched Capacitor , Switched Capacitor Filters.	12	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6026	Embedded Product Design	3-0-0-3		2015

Course Objectives

1. To learn about the systems engineering approach of embedded systems design.
2. To learn the concepts of product integrity, reliability and design analysis.
3. To have a basic exposure to the concepts of android based embedded system design and do a case study with reference to a 32 bit ARM architecture

Syllabus

Systems Engineering Approach to Embedded Systems Design, Embedded Hardware Building Blocks, Product Integrity and reliability, Design Analysis, Android based Embedded System Design, Case study with reference to a 32 bit ARM architecture.

Course Outcome

Students who successfully complete this course will be having the knowledge about the systems engineering approach of embedded systems design, product integrity, reliability and design analysis. Students should be able to contribute the knowledge in the design of embedded systems. Students will be able to involve in the design of android based embedded systems with the help of the concepts discussed in the syllabus and will also get an opportunity to do the case study on the representative embedded system discussed, with reference to 32 bit ARM architecture,to better understand the concepts.

Text Book

1. Tammy Noergaard, "Embedded Systems Architecture", Elsevier , 2005.
2. Project management of Complex and Embedded Systems Kim H Pries and Jon M Quigley, Auerbach Publications,2008.
3. The Design Analysis Handbook A Practical Guide to Design Validation , N Edward Walker, 2nd Edition, Newnes, 1998.
4. Embedded Android, KarimYaghmour, O'Reilly, 2011

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	A Systems Engineering Approach to Embedded Systems Design: Embedded system design, Life-Cycle Models, Embedded Systems Model, Standards diagram, Examples of standards implemented in embedded systems, Garbage Collection, Just in Time Compilation. Embedded Hardware Building Blocks and the Embedded Board: Different types of engineering hardware drawings, Timing diagrams, Schematic diagram –example, conventions and rules. Embedded Board - Major hardware components of boards, Embedded system board organization, Embedded reference board	10	25

	examples – x86 and ARM, Powering the Hardware.		
II	Product Integrity and reliability: Engineering issues, Production issues, Quality issues. Product Development: Product Development Overview, Delivery.	10	25
	INTERNAL TEST 1		
	Product Integrity and reliability, Cost. Process Development: Process Development overview, Product Integrity and reliability, Cost.		
III	Introduction to Design Analysis: Overview of the Design Validation Process, Quality Process Tree, Design Validation Tree. Traditional worst case analysis, Enhanced worst case analysis.Design Validation: Screening the analysis, Computer aided WCA, Software Analysis. Safety Analysis: Single point failure analysis, The Fault Tree analysis, The Sneak Path analysis.Electronic Analysis: Power and Thermal, Power Supplies, Grounding and Layout, EMI Noise Control	10	25
	INTERNAL TEST 2		
IV	Android based Embedded System Design: The Android Operating System: Introduction to Android technology, Open Handset Alliance, Getting "Android", Hardware and Compliance Requirements, Android Concepts, Framework Intro, App Development Tools, Native Development, Overall Architecture. Android Open Source Project, Getting AOSP, Build basics, Building Android, Running Android. Case study: With reference to a 32 bit ARM architecture, Android Based Smart Home Automation system - design from requirement analysis through concept design, detailed hardware and software design.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6036	**VLSI DESIGN AUTOMATION**	**3-0-0-3**		2015

Course Objectives

1. To learn basic concepts and flow in hardware design
2. To learn fundamental algorithms in physical design
3. To have a basic exposure to physical design automation, optimization techniques and data structures inside modern VLSI tools

Syllabus

Graph Algorithms, Logic Synthesis, High Level Synthesis, Compaction, Partitioning, Placement, Floorplanning, Pin Assignment, Global Routing, Detailed Routing

Expected outcome

At the end of the course, student will know the different stages of design flow; the basic data structures and algorithms used in each stage; and will be able to understand data structures and algorithms used in recent CAD tools; choose suitable data structures and propose new algorithms for CAD applications and develop new CAD tools

Text Books

1. Gerez,Sabih H., "Algorithms for VLSI Design Automation", John Wiley & Sons, 2006.
2. Sherwani, Naveed A., "Algorithms for VLSI Physical Design Automation*",*Kluwer Academic Publishers, 1999.

References

1. Meinel, Christoph, and Thorsten Theobald, "Algorithms and DataSstructures in VLSI Design: OBDD-Foundations and Applications*",*Springer-Verlag Berlin Heidelberg, 1998.
2. Drechsler, Rolf, "Evolutionary Algorithms for VLSI CAD" Springer Science & Business Media, 1998.
3. Trimberger, Stephen M., "An Introduction to CAD for VLSI", Springer Science & Business Media, 1987.
4. Sadiq M. Sait and H. Youssef, "VLSI Physical Design Automation: Theory and Practice", World Scientific, 1999.
5. Cormen, Thomas H., Charles E. Leiserson, and Ronald L. Rivest. "Introduction to Algorithms." The MIT Press, 3rd edition, 2009.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	**Graph Algorithms:** Data structures for Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm - Kruskal's and Prim's, Shortest path Algorithm - Dijkstra's Algorithm for single pair Shortest path, Floyd-Warshall algorithm for All pair Shortest path, Min cut and Max cut Algorithms	10	

II	**Logic Synthesis:** Introduction to Combinational Logic Synthesis, Binary Decision Diagrams. **High Level Synthesis:** Hardware models for High-level synthesis, Internal Representation of the Input Algorithm, Allocation , Assignment and Scheduling, ASAP Scheduling, Mobility-Based Scheduling, Force-Directed Scheduling, List Scheduling.	10	
	INTERNAL TEST 1		
	Compaction: Problem Formulation, Longest Path Algorithm for DAGs – without cycles and with cycles, Liao-Wong Algorithm, Bellman-Ford Algorithm.		
III	**Partitioning:**Kernighan-Lin Partitioning Algorithm, Fiduccia-Mattheyses Algorithm. **Placement:** Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms – Constructive Placement, Iterative Improvement. **Floorplanning:**Floorplan Representation, Shape Functions, Floorplan Sizing. **Pin Assignment:** Problem Formulation, General Pin Assignment, Channel Pin Assignment.	10	
	INTERNAL TEST 2		
IV	**Global Routing:** Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithm – Lee's Algorithm, Line-Probe algorithm, Steiner Tree based Algorithm. **Detailed Routing:** Area Routing, Channel Routing – Channel Routing Model, Vertical and Horizontal Constraint Graph, Left-edge Algorithm, Robust Channel Routing Algorithm.	10	
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6146	System on Chip Design	3-0-0-3		2015

Course Objectives

1. To learn about the system on chip design process and macro design process.
2. To learn the concepts of system on chip verification technology options.
3. To have a basic exposure to the concepts of multi-processor system on chips and the techniques for designing MPSoCs.

Syllabus

System On Chip Design Process, Macro Design Process,SoCverification technology options, Multi-processor System on Chipsand the techniques for designing MPSoCs.

Course Outcome

Students who successfully complete this course will be having the knowledge about the system on chip design process and the macro design process.Students should be able to contribute the knowledge in system on chip design process. Students will also learn about SoCverification technology options and the techniques for designing MPSoCs.

Text Book

1. Michael Keating, Pierre Bricaud,Reuse Methodology manual for System-On-A-Chip Designs,Kluwer Academic Publishers,second edition,2001
2. PrakashRashinkar, Peter Paterson and Leena Singh, SoC Verification-Methodology and Techniques, Kluwer Academic Publishers,2001.
3. A.A.Jerraya, W.Wolf, Multiprocessor Systems-on-chips, 1st Edition,Morgan Kaufmann, 2004.

References

1. William KLam, Design Verification:Simulation and Formal Method based Approaches,1st Edition, Prentice Hall, 2005.
2. RochitRajsuman, System-on-a-Chip-Design and Test,Artech House, 2000.
3. Dirk Jansen ,The Electronic Design Automation Handbook , Springer, 2003.

Course Plan			
Module	Content	Hours	Sem. Exam Marks
I	System On Chip Design Process: A canonical SoC Design, SoC Design flow - waterfall vs spiral, Top-down vs Bottom up, Specification requirement, Types of Specification, System Design process, System level design issues- Soft IP vs Hard IP, Design for timing closure, Logic design issues- Verification strategy, On-chip buses and interfaces, Low Power, Manufacturing test strategies.	10	25
II	Macro Design Process: Top level Macro Design, Macro Integration, Soft Macro productization.	10	25
	INTERNAL TEST 1		
	Developing hard macros, Design issues for hard macros, Design process, System Integration with reusable macros.		
III	SoC Verification:-Verification technology options, Verification methodology, Verification languages,Verification approaches, and Verification plans. System level verification, Block level verification,Hardware/software co-verification and Static net list verification.	10	25
	INTERNAL TEST 2		
IV	MPSoCs: What, Why, How MPSoCs. Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design, MPSoC performance modeling and analysis. System-In-Package (SIP) design.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6246	**FPGA ARCHITECTURE & APPLICATIONS**	**3-0-0-3**		**2015**

Pre-requisites: Fundamentals ofDigital Design, One hardware description Language Verilog/VHDL

Course Objectives

To give the Student an idea about:-

1. FPGA evolution, its usefulness and architecture.
2. FPGA technology, the design process and how the design is mapped to the existing hardware in FPGA.
3. How to implement arithmetic using FPGA which is a must for computationally intensive high end applications.
4. FPGA applications through a case study.
5. Reconfigurable computing systems and architecture.

Syllabus

FPGA evolution and architecture using an example. Review of concepts of Logic Design pertaining to FPGA and design flow. Arithmetic implementation and reconfigurable computing using FPGAs.

Course Outcome

Students who successfully complete this course will demonstrate an ability to design a system using FPGAs; understand the logic design concept pertaining to FPGA and how a design will be mapped to FPGA. The students will demonstrate an understanding of design flow to program an FPGA. The students will equip with the capability of implementing any computationally intensive algorithm in FPGA. The students will demonstrate capability to understand high end systems with

reconfigurable concepts.

Text Book

1. P.K.Chan& S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. Reconfigurable Computing: The Theory and Practice of FPGA based Computation, Scott Hauck and Andre De Hon, Morgan Kaufmann Publishers,2007

References

1. S. Trimberger, Edr. Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
2. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, Reprint 2008.
3. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, BSP, 2007.
4. Jean-Pierre Deschamps and Gustavo D. Sutter, Guide to FPGA Implementation of Arithmetic Functions, 2009.
5. S. Brown and J. Rose, "Architecture of FPGAs and CPLDs: A Tutorial", IEEE Design & Test of Computers, Vol. 13, No. 2, pp. 42-57, 1996.
6. Digital Systems Design with FPGA's and CPLDs – Ian Grout, Elsevier, 2009

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	RAM ROM PLA PAL PGA, CPLD: overview, Features and Applications FPGA Architecture: overview, Xilinx Logic Cell Array, Configurable Logic Block, I/O Block, Programmable Interconnects, Programming methods Advanced features of Xilinx 4000 series Technology Trends:Device capacity, Utilization and Gate Density, Programming methods, General Design Flow: General Design Guidelines	10	25

	Case Studies-FPGA: Xilinx Virtex-6, Spartan-6 Advanced features in FPGA based on Case studies		
II	Review of Logic Design: Boolean Algebra, Designing with complete Gates, Minimization of combinational Functions, QuineMcClusky Algorithm Multilevel Logic Minimization: Representation of Boolean Functions, Multilevel Logic Minimization Methods, Technology mapping: Relating literal Counts to number of CLBs: Finite State machines: One hot, basic architecture, Advantages, disadvantages Case Study: Simple Static RAM tester	10	25
	INTERNAL TEST 1		
	Petri nets for State machines: basic architecture Placement and Routing: Verification and Testing:		
III	FPGA Implemention of Arithmetic: Adders, Substractors, Dividers, Multiplier, Converters, Square Root, Logarithmic, Trignometric, Floating Point, Finite Field Arithmetic, Case Study: CORDIC Architectures for FPGA Computing: CORDIC Algorithm, Architectural Design, FPGA Implementation of CORDIC Processors	10	25
	INTERNAL TEST 2		
IV	Reconfigurable computing: Reconfigurable computing systems, Reconfigurable computing architectures, Reconfiguration management, System architectures, Case Study: Automatic Target Recognition Systems on Reconfigurable Devices	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6346	VLSI ARCHITECTURES FOR DSP	3-0-0-3		2015

Course Objectives

To give the Student an idea about:-

1. The graph representations of DSP algorithms, Convolution algorithms.
2. The concept of parallel recursive and adaptive filters.
3. The idea of scaling and round off noise and about digital lattice filter structures

Syllabus

Block Diagram and Graph Representations of DSP Algorithms, Pipelining and Parallel processing of filters, Fast convolution, Parallel FIR filters, Scaling and Round off noise, State variable description of Digital Filters, Digital lattice filter structures.

Course Outcome

At the end of the course, student will know about the graph representations of DSP algorithms, Convolution algorithms and the concept of parallel recursive and adaptive filters. Students should be able to contribute the knowledge in the design ofparallel recursive and adaptive filters. Students will also be able to understandstate variable description of digital filters and digital lattice filter structures.

Text Book

1. VLSI DSP Systems- Design and Implementation – Keshab K Parhi, John Wiley, 2004.
2. Digital Signal Processing with Field Programmable Gate Arrays - Uwe Meyer Baese, Springer Verlag 2001.
3. Digital Signal Processors : Architectures , Implementations and applications, Sen M Kuo, Woon-Seng S. Gan, Prentice Hall, 2004
4. DSP integrated circuits, Lars Wanhammar, Academic Press, 1999.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Block Diagram and Graph Representations of DSP Algorithms – Signal Flow Graph, Data Flow Graph and Dependence Graphs – Algorithms for Shortest Path Computation - Pipelining and Parallel processing of filters - - Pipelining and parallel processing for Low Power.Retiming - Definitions and Properties - solving system of inequalities - Retiming techniques.Unfolding - algorithm for unfolding - Properties of unfolding - Critical path, Unfolding and retiming – Applications. Folding - Folding transformation -	10	25

	Register minimization techniques - Register minimization in folded architectures.		
II	Fast convolution – Cook Toom and Winograd Algorithms – Modified Algorithms - Iterated convolution - Cyclic convolution - Algorithmic strength reduction in filters and transforms - Parallel FIR filters - Pipelined and parallel recursive and adaptive filters	10	25
	INTERNAL TEST 1		
	Pipeline interleaving in Digital filters - Pipelining in IIR digital filters - Parallel processing for IIR filters - Low power IIR filter design using Pipelining and Parallel processing.		
III	Scaling and Round off noise – Scaling and Round off noise - State variable description of Digital Filters - Scaling and Round off noise computation - Round off noise in Pipelined IIR filters - Round off noise computation using state variable description - SRP Transformation.	10	25
	INTERNAL TEST 2		
IV	Digital lattice filter structures - Schur Algorithm - Digital basic lattice filters, Derivation of one multiplier Lattice filter - Derivation of scaled-normalized lattice filter - Round off noise calculation in Lattice filters. Bit level arithmetic architectures - Parallel multipliers - Bit serial filter design and implementation - Canonic signed digital arithmetic.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6156	Embedded Linux Systems	3-0-0-3		2015

Course Objectives

To give the Student an idea about:-

1. Embedded Linux systems and the set up of cross platform tool chains.
2. Kernel and Root Filesystem set up.
3. Root Filesystem Setup and the boot loader configurations
4. Device drivers.

Syllabus

Embedded Linux systems, Cross platform development toolchain setup for Embedded Linux Systems, Kernel and Root File System configuration, Bootloader Configuration and the concept of device drivers.

Course Outcome

After the successful completion of the course, students will be having the knowledge aboutEmbedded Linux systems, and the platform setup for bringing up Embedded Linux systems.Students should be able to contribute the knowledge in Embedded Linux Systems. Students will also learn about the ways to configure the kernel, configure the Root File System, configure the bootloader and will demonstrate capability to understand device drivers.

Text Book

1. Building Embedded Linux Systems , KarimYaghmour, JonJasonBrittain and Ian F. Darwin Masters, Gilad Ben-Yossef, and Philippe Gerum, 2nd Edition, O'Reilly, 2008
2. Linux Device Drivers , Alessandro Rubini, Jonathan Corbet, 3rd Edition,O'Reilly, 2005

References

1. Embedded Linux Primer A Practical Real – World Approach, Christopher Hallinan, 1st Edition, Prentice Hall, 2006
2. Embedded Linux System Design and Development , P Raghavan, Amol Lad, SriramNeelakandan , CRC Press, 2005
3. Essential Linux Device Drivers , Alan Cox, Sreekrishnan , Venkateswaran , 1st Edition, Prentice Hall, 2008
4. Craig Hollabaugh, Embedded Linux - Hardware, Software and Interfacing, Pearson Education, 2002

Course Plan

Module	Content	Hours	Sem. Exam Marks

<table>
<tr><td>I</td><td>Introduction: Embedded Linux, Real Time Linux,Types of Embedded Linux systems, Advantages of Linux OS, Using distributions, Examples of Embedded Linux systems- system architecture, Types of host/target architectures for the development of Embedded Linux Systems, Debug setups, Boot Configurations, Processor architectures supported by Linux.</td><td>10</td><td>25</td></tr>
<tr><td rowspan="3">II</td><td>Cross platform Development toolchain: GNU tool chain basics, Kernel Headers Setup, Binutils setup, Bootstrap Compiler Setup, Library Setup, Full Compiler Setup, Using the tool chain.</td><td rowspan="3">10</td><td rowspan="3">25</td></tr>
<tr><td>INTERNAL TEST 1</td></tr>
<tr><td>C library alternatives, JAVA, Perl, Python, Ada, IDEs , Terminal Emulators.</td></tr>
<tr><td rowspan="2">III</td><td>Kernel and Root File System, Kernel Considerations- selection, configuration , Compiling and Installing the kernel Root File System Structure, Librariries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization.Storage Device Manipulation. MTD-Supported Devices ,Disk Devices, Swapping.</td><td rowspan="2">10</td><td rowspan="2">25</td></tr>
<tr><td>INTERNAL TEST 2</td></tr>
<tr><td>IV</td><td>Root FilesystemSetup :Filesystem Types for Embedded Devices, Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem, Placing a Disk Filesystem on a RAM Disk, Rootfs and Initramfs, Choosing a Filesystem’s Type and Layout, Handling Software Upgrades. Setting Up the Bootloader Embedded Bootloaders, Server Setup for Network Boot,Using the U-Boot Bootloader.Device Drivers: Introduction, Building and running modules, Char Drivers, USB Drivers, Block Drivers.</td><td>10</td><td>25</td></tr>
<tr><td colspan="4">END SEMESTER EXAM</td></tr>
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Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6256	**Modeling of Embedded Systems**	**3-0-0-3**		**2015**

Course Objectives

To give the Student an idea about:-

1. Provide an understanding of the need for modelling
2. Introduce and expose students with the fundamental concepts of modelling Embedded Systems
3. To link the studied concepts with real life applications.

Syllabus

Introduction, System Design Methodologies & Models; Software and hardware synthesis; Verification.

Course Outcome

Students who successfully complete this course will be able to understand the need for modelling, Well verse with the concepts of modelling, Gain familiarity with system level design tools & their design flow of academic tools ,gain familiarity with embedded s/w design tools &the tool flow , gain familiarity with hardware design tools & their design flow.

Text Book

1. Daniel D. Gajski , Samar Abdi Andreas and GerstlauerGunarSchirner , "Embedded System Design Modeling, Synthesis & Verification", Springer, 2009
2. A. Jantsch, Morgan , "Modeling Embedded Systems and SoCs - Concurrency and Time in Models of Computation", Kaufmann, 2003.
3. Gomaa , "Software Design Methods for Concurrent and Real-time Systems",
4. Henzinger, T., Sifakis, J, The Discipline of Embedded System Design, Addison-Wesley1993
5. Tony D. Givargis, Embedded System Design: A Unified Hardware/Software Introduction, Frank Vahid and, 2000
6. Wayne Wolf , Computers as Components-principles of Embedded computer system design, Elseveir, 2005
7. J. Banks, J. S. Carson II, B. L. Nelson, and D. M. Nicol,Discrete-Event System Simulation Prentice-Hall, 2001.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Introduction, System Design Methodologies & Models: - System-Design Challenges Abstraction Levels ,System Design Methodology, System-Level Models Platform Design System Design Tools. System Design Methodologies- Bottom-up	10	25

	Methodology, Top-down Methodology, Meet-in-the-middle Methodology Platform Methodology Field Programmable Gate Array(FPGA) Methodology System-level Synthesis Processor Synthesis. Models-Models of Computation, System Design Languages, System Modeling, Processor Modeling, Communication Modeling, System Models.		
II	System Synthesis:-System Design Trends, Transaction Level Model(TLM) Based Design, Automatic TLM Generation, Automatic Mapping Platform Synthesis.	10	25
	INTERNAL TEST 1		
	Software synthesis- Preliminaries, Software Synthesis Overview, Code Generation, Multi-Task Synthesis, Internal Communication, External Communication, Startup Code, Binary Image Generation Execution.		
III	Hardware synthesis:- Register Transfer Logic(RTL) Architecture, Input Models Estimation and Optimization, Register Sharing, Functional Unit Sharing, Connection Sharing, Register Merging, Chaining and Multi-Cycling, Functional-Unit Pipelining, Datapath Pipelining, Control and Datapath Pipelining, Scheduling Interface Synthesis.	10	25
	INTERNAL TEST 2		
IV	Verification:- Simulation Based Methods, Formal Verification Methods, Comparative Analysis of Verification Methods, System Level Verification . Embedded Design Practise -System Level Design Tools, Embedded Software Design Tools, Hardware Design Tools, Case Study.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC6356	MOBILE HANDSET ARCHITECTURE	3-0-0-3		2015

Course Objectives

1. To understand the basics of mobile communication systems
2. To learn various hardware and software design perspectives of mobile Handsets
3. To understand the architecture of common hardware and software components used inside modern mobile handsets.
4. To learn about the future handset design technologies and protocols.

Syllabus

Introduction to mobile communication & mobile handset design, Hardware Architecture of mobile handsets, Designing of mobile handset software, Product Design & Future Handset Designs.

Course Outcome

At the end of the course, student will be able to evaluate the various design methodologies involved in mobile handset design and to select the most optimal one ;
To select the optimal hardware and software components for a given mobile phone design specification;
To design and evaluate mobile handset hardware and software architectures.

Text Book

1. Abhi Naha & Peter Whale, " Essentials of Mobile handset Design ", Cambridge University Press, August 2012.
2. Sajal Kumar Das, "Mobile Handset Design", John Wiley & sons,2010.

References

1. Reto Meier, "Professional Android 4 Application Development (Wrox)", John Wiley & sons,2012.
2. PattnaikPrasantKumar , Mall Rajib , "Fudamentals of Mobile Computing", PHI, 2012.
3. Asoke K. Talukdar , "Mobile Computing", Second Edition, McGraw Hill,2010.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Introduction to mobile communication & mobile handset design. Introduction to mobile handsets:- Basic Elements of Telecommunication & Wireless Telecommunication Systems , Generation of Electromagnetic Carrier Waves for Wireless Communication , Concept of the Antenna, Basic Building Blocks of a Wireless Transmitter and Receiver ,The Need for a	10	25

	Communication Protocol, Evolution of Wireless Communication Systems ,Low Mobility Supported Wireless Phones ,Cellular Mobile Communication & Mobile Handsets Beginnings & Timeline of the mobile phone ,Various Design perspectives , Hardware Design -The radio spectrum Radio chipset design Digital chipset design Baseband cellular modem design Mobile application processor design Multimedia processor design Peripheral component design		
II	Hardware Designing of mobile handset. Anatomy of a GSM mobile handset :- Functional Blocks Inside a GSM Mobile Phone, Hardware Block Diagram of a Mobile Phone ,GSM Transmitter and Receiver Module , Antenna ,Analog to Digital Conversion (ADC) Module ,Automatic Gain Control (AGC) Module, Automatic Frequency Correction Module, Loudspeaker, Microphone (MIC) , Subscriber Identity Module (SIM), Application Processing Unit, Camera, LCD Display Keypad, **INTERNAL TEST 1** Connectivity Modules -Bluetooth &USB, Battery- Primary Cells Rechargeable Battery Types , Battery Charger Circuit ,Sleep Mode, Clocking Scheme, Alert Signal Generation, Memory -Read Only Memory (ROM) ,Flash Memory , Random Access Memory (RAM) GSM Receiver Performance. Architecture of (Block Level Only) Qualcomm Snapdragon S1, Samsung Exynos 3 single and NvidiaTegra 2 processors. Case Study of any one of the above Mobile SoCs.	10	25
III	Software Design of mobile handset. GSM Mobile Phone Software Design -Boot Loader and Initial Power on Software Module, Operating System Software, Device Driver Software,GSM System Protocol Software -GSM Mobile Handset (MS) Protocol Stack , Air Interface (Um) Protocol ,Abis Interface & A Interface ,Speech and Multimedia Application Software -Speech Codec, Audio Codec, Image & Video. Application software design Protocol stack software design Physical layer software design Mobile operating systems and execution environments. Case Studies (Mobile Operating Systems) :- – Android and Apple iOS **INTERNAL TEST 2**	10	25

IV	Product Design& Future Handset Designs. Product design The design process -Industrial design Mechanical design engineering Hardware design engineering Software platform design , Manufacturing production Testing and qualification Case study:- Capacitive touchscreens in mobile handsets . Anatomy of a UMTS Mobile Handset - Mobile System Architecture, UE Hardware Architecture and Components, Multirate User Data Transmission, Implementation of UE System Procedures Design of the UMTS Layer-1 Operation States .Next Generation Mobile Phones- Introduction, 3GPP LTE , LTE System Design ,IEEE 802.16 System ,4G Mobile System, Key Challenges in Designing 4G Mobile Systems, Cognitive Radio Competitive Edge in Mobile Phone System Design - Key Challenges in Mobile Phone System Design ,System Design Goal,Protocol Architecture Design Optimization,Hardware/Software Partitioning ,System Performance, Adaptability ,Verification, Validation and Testing , Productization.	10	25
END SEMESTER EXAM			

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC6066	MINI PROJECT	0-0-4-2	2015

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC6076	VLSI& Embedded Systems Design Lab II	0-0-3-1	2015

Digital Circuit Design

Physical Design of digital logic circuits

Interfacing of FPGAs with external logic with the help of soft processors/IP cores

Analog Circuit Design

Spice analysis of differential amplifiers and operational amplifiers

Layout design and analysis of Analog Integrated Circuits

Embedded Design Lab

OS porting to Embedded platform

Application development

SEMESTER-III

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC7115	High Speed Digital Design	3-0-0-3		2015

Course Objectives

To give the Student an idea about:-

1. To learn the fundamentals of High speed signal propagation in circuits and cables.
2. To understand the principles of signal integrity and its applications in the proper design of high-speed digital circuits.
3. To have a basic exposure to the different conventions and modelling schemes used in High Speed Digital Design Circuits.

Syllabus

Introduction to High Speed Digital Design, Modeling of Wires, Power Distribution, Noise Sources in Digital Systems, Signaling Conventions, Terminator Circuits, Timing Convention, Clock Distribution and Synchronization.

Course Outcome

At the end of the course, student will know the fundamentals of high speed signal propagation in circuits and cables; the practical and theoretical aspects necessary to design modern High Speed Digital systems at the platform level; and will be able to apply this knowledge to determine where signal integrity issues may arise and how to solve problems of poor digital signal integrity.

Text Book

1. Dally &Paulton, Digital System Engineering, Cambridge University Press, 1998.
2. Johnson & Graham, High Speed Digital Design: A Handbook of Black Magic, Prentice Hall 1993.

References

1. Meinel, Christoph, and Thorsten Theobald, "Algorithms and Data Structures in VLSI Design: OBDD-Foundations and Applications", Springer-Verlag Berlin Heidelberg, 1998.
2. Drechsler, Rolf, "Evolutionary Algorithms for VLSI CAD" Springer Science & Business Media, 1998.
3. Masakazu Shoji, High Speed Digital Circuits, Addison Wesley, 1996.
4. Jan M.Rabaey et al. Digital Integrated Circuits: A design Perspective, 2003.

Course Plan

Module	Content	Hours	Sem. Exam Marks

I	**Introduction to High Speed Digital Design:** Frequency, time and distance, Knee Frequency and its significance, Propagation Delay, Capacitance and Inductance Effects, High speed properties of logical gates, Speed and power. **Modeling of wires:**Geometry and Electrical properties of wires, Electrical model of wires. **Transmission Lines:**Lattice Diagram Analysis of Transmission Lines, Simple and Special Transmission Lines.	10	25
II	**Power Distribution:** Power supply network, Local power regulation, IR drops, Area bonding, On chip bypass capacitors, Bypass Capacitor Design, Symbiotic bypass capacitors, Power supply isolation.	10	25
	INTERNAL TEST 1		
	Noise sources in digital system: Power supply Noise, Cross talk, Intersymbol Interference.		
III	**Signaling conventions:**Signaling modes for transmission lines, Signaling over lumped transmission media, Signaling over RC interconnects, driving lossy LC lines, simultaneous bi-directional Signaling. **Terminator Circuits:** Transmitter and receiver circuits.	10	25
	INTERNAL TEST 2		
IV	**Timing Convention:** Timing fundamentals, Timing properties of clocked storage elements, signals and events, Open loop Timing, level sensitive clocking, Pipeline Timing, Closed loop Timing, **Clock Distribution and Synchronization:** Clock Distribution, Synchronization failure and Metastability, PLL and DLL based clock aligners.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC7215	MEMS & MICRO SYSTEM DESIGN	3-0-0-3		2015

Course Objectives

1. To learn the fundamentals of MEMS & Micro System Design.
2. To present a general introduction to the field of MEMS, with emphasis on its commercial applications and device fabrication methods.
3. To learn about the new materials, science and technology for microsystem applications..

Syllabus

History of MEMS, MEMS materials, MEMS fabrication processes, Micromachining, MEMS Devices & Packaging, MEMS Packaging issues, Application Case studies.

Course Outcome

At the end of the course, student will know the fabrication technologies; material properties and structural mechanics; packaging, and MEMS markets and applications; and will be able to understand state-of-the-art micromachining and packaging technologies.

Text Book

1. Foundation of MEMS, Second Edition 2011 – Chang Liu, Pearson.
2. Gregory T A, Kovacs Micro machined Transducers Sourcebook, WCB McGraw-Hill, 1998.

References

1. Microsystem Design – by Stephen D. Senturia, Publishers: Kluwer Academic / Springer, 2nd Edition (2005), ISBN: 0792372468
2. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 2002.
3. NadimMaluf, An introduction to Microelectromechanical system design, ArtechHouse, 2000
4. Mohamed Gad-el-Hak, Editor, The MEMS Handbook, CRC Press, Baco Raton, 2002.

Course Plan

Module	Content	Hours	Sem. Exam Marks

I	History of MicroElectroMechanical Systems (MEMS), market for MEMS, MEMS Materials: Silicon and other materials , mechanical properties of materials- elasticity, stress and strain, Beams & Structures –cantilevers and bridges, point load & uniform loading, torsional, dynamic system; Piezoelectric &piezoresistive materials.	10	25
II	MEMS fabrication processes: Review of IC fabrication process, Micromachining: Bulk micromachining (dry and wet etching).	10	25
	INTERNAL TEST 1		
	Surface micromachining (deposition, evaporation, sputtering, epitaxial growth), Deep RIE, Advanced Lithography, LIGA process; Multi User MEMS Process.		
III	MEMS Devices & Packaging: MEMS Sensors and Actuators (Electrostatic, Electromagnetic, Thermal and Piezo), Bio-MEMS, Optical MEMS, Micro-fluidics MEMS; MEMS packaging issues, die-level packaging, micro assembled caps & sealing.	10	25
	INTERNAL TEST 2		
IV	Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD), Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT), Air bag system, Micromotors, Scanning Probe Microscopy.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC7315	**DSP Architecture and Design**	**3-0-0-3**		**2015**

Course Objectives

To give the Student an idea about:-

1. Hardware modeling, DSP algorithms and architecture design and DSP module synthesis.
2. To present a general introduction toDSP algorithm and architecture design and VLSI performance measures.
3. To introduce the concept of parallel algorithms and their dependence.

Syllabus

Hardware modelling, DSP Algorithm and Architecture Design, VLSI performance measures (area, power, and speed), structural modeling in VHDL, High performance arithmetic unit architectures, DSP Module Synthesis, Parallel algorithms and their dependence, Applications using common DSP algorithms.

Course Outcome

Students who successfully complete this course will be having the knowledge abouthardware modelling, DSP algorithm and architecture design and DSP Module Synthesis.Students should be able to contribute the knowledge in DSP architecture design. Students will be able to understand the concept of parallel algorithms and their dependence and applications.

Text Book

1. SenM.Kuo ,Woon-Seng S. Gan, Digal Signal Processors: Architectures, Implementations, and Applications Prentice Hall 2004.
2. Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Array, Springer-Verlag 2001.
3. Keshab K. Parhi, VLSI Signal Processing Systems, Design and Implementation, John Wiley & Sons,1999.
4. John G. Proakis ,DimitrisManolakis K, DSP Principles, Algorithms and Applications, Prentice Hall 1995.

5. J Bhasker, VHDL Primer, Pearson Education Asia, 3rd edition.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	Hardware modeling: Introduction to hardware description language, hardware abstraction, entity declaration, architecture body, behavioralmodeling, process statement, signal assignment statement, dataflow modeling, concurrent signal assignment statement, structural modeling, component declaration, component instantiation statement, mixed modeling, Case study: mixed style of modeling of a full adder, modeling of a state register.	10	25
II	DSP Algorithm and Architecture Design: DSP representations (data-flow, control-flow, and signal-flow graphs, block diagrams), filter structures (recursive, non recursive and lattice), behavioralmodeling in HDL, system modeling and performance measures,	10	25
	INTERNAL TEST 1		
	Fast filtering algorithms (Winograd's, FFT, short- length FIR), retiming and pipelining, block processing, folding, distributed arithmetic architectures, VLSI performance measures (area, power, and speed), structural modeling in VHDL.		
III	DSP Module Synthesis: distributed arithmetic (DA), advantageous of using DA, size reduction of look-up tables, canonic signed digit arithmetic, implementation of elementary functions Table-oriented methods, linear feedback shift register, high performance arithmetic unit architectures (adders, multipliers, dividers), bit-parallel, bit-serial, digit-serial, carry-save architectures, redundant number system, modeling for synthesis in HDL, synthesis place-and-route.	10	25
	INTERNAL TEST 2		
IV	Parallel algorithms and their dependence: Applications to some common DSP algorithms, system timing using the scheduling vector, projection of the dependence graph using a projection direction, the delay operator and z-transform techniques for	10	25

	mapping DSP algorithms onto processor arrays, algebraic technique for mapping algorithms, computation domain, dependence matrix of a variable, scheduling and projection functions, data broadcast and pipelining, applications using common DSP algorithms.		

END SEMESTER EXAM

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC7125	**Low Power Digital Design**	**3-0-0-3**		**2015**

Course Objectives

To give the student an idea about:-

1. The need for low power VLSI chips, sources of power dissipation on digital integrated circuits and emerging low power approaches.
2. The concept of simulation power analysis and circuit level low power design.
3. The concept of low power architecture & systems.

Syllabus

Need for low power VLSI chips, sources of power dissipation on digital integrated circuits, emerging low power approaches, simulation power analysis, circuit level low power design, low power architecture & systems.

Course Outcome

Students who successfully complete this course will be having the knowledge about low power VLSI chips, sources of power dissipation on digital integrated circuits and emerging low power approaches. Students should be able to contribute the knowledge in the design of low power VLSI chips and in the design of low power memory. Students will also be able to understand the concept of simulation power analysis and circuit level low power design.

Text Book

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

References

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000

Course Plan

Module	Content	Hours	Sem. Exam Marks

I	Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. Device & Technology Impact on Low Power, Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. Power estimation.	10	25
II	Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems.	10	25
	INTERNAL TEST 1		
	Monte Carlo simulation.Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.		
III	Low Power Design- Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, precomputation logic	10	25
	INTERNAL TEST 2		
IV	Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC7225	**VLSI SYSTEM TESTING**	**3-0-0-3**		**2015**

Course Objectives

1. To learn fault modelling and fault detection
2. To learn concepts of test generation for combinational and sequential circuits
3. To learn hardware design for testing
4. To introduce concepts of fault diagnosis

Syllabus

Introduction to Testing, Simulation, Testability Measure, Combinational & Sequential ATPG, Memory Test, Delay Test, IDDQ Test, DFT, BIST, Diagnosis.

Course Outcome

At the end of the course, student will know the concepts of manufacturing testing; select the fault model and test strategy for a test environment; generate test vectors depending on the fault model; design hardware to enhance testability of the system; design hardware test generation.

Text Book

1. Viswani D Agarwal and Michael L Bushnell, "Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits", Springer, 2000.
2. 2. M. Abramovici, M A Breuer and A D Friedman, "Digital systems Testing and Testable Design", IEEE Press, 1994.

References

1. Alfred L Cronch, "Design for Test for Digital IC's and Embedded Core system", Prentice Hall, 1999.
2. NirajJha and Sanjeep K Gupta, "Testing of Digital Systems", Cambridge University Press, 2003.
3. L-T Wang, C-W Wu, and X. Wen "VLSI Test Principles and Architectures: Design for Testability", Academic Press, 2006.

Course Plan

Module	Content	Hours	Sem. Exam Marks
I	**Introduction to Testing**: Role of Testing, Yield, ATE Block Diagram, Fault Modeling, Glossary of Fault Models, Single Stuck-at-Faults, Functional Equivalence, Fault Collapsing, Dominance,	10	25

	Check Point Theorem **Simulation**: Logic and Fault Simulation, ModelingSignalStates, Algorithm for True Value Simulation, Algorithm for FaultSimulation, Serial and Parallel Fault Simulation		
II	**Testability Measures**: Combinational SCOAP Measures – Sequential SCOAP Measures.	10	25
	INTERNAL TEST 1		
	Combinational ATPG: Boolean Difference Method, D-Algorithm, PODEM, FAN **Sequential ATPG**: Time-Frame Expansion Method, Simulation Based Methods		
III	**Memory Test**: Faults, Fault Modelling, March Test **Delay Test**: Path Delay Test, Transition Faults, Delay Test Methodologies, At-Speed Testing **IDDQ Testing**:Faults, IDDQ Testing Methods	10	25
	INTERNAL TEST 2		
IV	**Design for Testability**: Ad-Hoc DFT Methods, Scan design, Partial Scan Design, Random Access Scan **Built-In Self-Test**: Random BIST - Memory BIST, Boundary Scan Standard **Diagnosis**: Introduction to Fault Diagnosis and Self-checking Design.	10	25
END SEMESTER EXAM			

Course Code	Course Name	L-T-P-C		Year of Introduction
06EC7325	**Memory Design & Testing**	**3-0-0-3**		**2015**

Course Objectives

This course gives an idea about different types of memories, its architecture and technologies used in the industry. How to design for testing and to create a good fault model for successful testing is looked into. The course also takes one through reliability and effect of radiation and the advanced memory technologies and packaging.

Syllabus

Different types of memories, random access and non-volatile. Fault modelling and design for testing. Reliability and radiation effects. Advanced memory technology and packaging.

Course Outcome

The student who successfully undergoes this course will have an idea about the different types of memories used in industry and its architecture and technologies used. The student will be able to demonstrate how to fault model different memories and demonstrate one's ability to design for testing. The student will be well versed with reliability issues in memories and also about the advanced technologies and packaging.

Text Book

1. A.K Sharma, " Semiconductor Memories Technology, Testing and Reliability", IEEE Press, 2002.
2. Luecke Mize Carr, " Semiconductor Memory design & application", Mc-Graw Hill, 1973
3. Belty Prince, " Semiconductor Memory Design Handbook
4. Memory Technology design and testing IEEE International Workshop on: IEEE Computer Society Sponsor (S), 1999

Course Plan

Module	Content	Hours	Sem. Exam Marks

I	Random Access Memory Technologies -Static Random Access Memories (SRAMs):SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology- Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.NonvolatileMemories Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One- Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.	10	25
II	Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance. RAM Fault Modeling.	10	25
	INTERNAL TEST 1		
	Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.		
III	Semiconductor Memory Reliability And Radiation Effects General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing – Radiation Dosimetry-Water Level Radiation Testing and Test Structures.	10	25
	INTERNAL TEST 2		
IV	Advanced Memory Technologies And High-Density Memory Packaging Technologies Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-	10	25

	Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.		
END SEMESTER EXAM			

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC7035	Seminar II	0-0-2-2	2015

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC7045	Project(Phase 1)	0-0-8-6	2015

SEMESTER-IV

Course No.	Course Name	L-T-P Credits	Year of Introduction
06EC7016	Project(Phase 2)	0-0-21-12	2015